#### **DESIGN FOR MANUFACTURING**

# **Considering Creepage and Clearance**

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Several years ago, my company published a guide to the design and manufacture of PCBs that would carry very high voltage, potentials up to 40,000V. Much of the advice in that brief regards a narrow project category, and I have an idea that a review of the basic layout precautions for any board that would carry what is considered hazardous voltage—greater than  $30V_{\text{RMS}}$ , or 60V dc—would have a much wider audience. Reiterating such rules now and again could save a lot of headaches and perhaps liability down the road.

If the system or product for which your board is destined must meet IEC or UL standards, the minimum distance permitted between conductors that are subject to hazardous voltage will include a wide margin for safety, which depends on the peak working voltage, laminate material, operating environment (moisture, particulates, altitude), circuit location relative to human access or proximity, and whether the traces involved are on an internal or outer layer. The spacing required on outer layers also depends on whether traces are coated or bare.

Determining what spacing to use is simple, if your system or product requires compliance to international safety standards. Find the standard relevant to the product category and adhere to the tabulated values with respect to the details of your application as noted. For example, IEC-60950-1 (2nd edition) is the document to consult for most IT products to be sold internationally that are powered from ac mains, or batteries, and applies both to the primary



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side and the dc secondary circuits within those products. Starting with section 2.10.3, midway through the document, the standard defines what clearances are required so that over-voltages, including transients and peak voltages that may be generated within the equipment,

cannot cause faults. A series of tables, 2J through 2M, explains how to calculate clearances with respect to the details of your application. Next, section 2.10.4 explains how to determine the spacing required for creepage.

#### **Clearance vs. Creepage**

What's the difference between clearance and creepage? Clearance is the shortest distance between two conductors measured through air. Creepage is the shortest distance betwo conductors, tween measured along the surface of the insulation separating them. Consider the ways an electrical fault between conductors can occur if the clearance or the creepage spacing is too small. If the clearance is too small, transient over-voltage а event can result in arcing between the conductors, especially if there is dust in the air or humidity. This is a virtually instantaneous fault that does not recur until another such overvoltage event. Faults resulting from insufficient spacing for creepage can take much longer to occur. Over time, usu-

ally stemming from dust buildup and moisture, a path (in other words, a track) for current to leak from one conductor to another can develop and cause a gradual breakdown of the surface of the insulating material between them. The mechanism for this is not a voltage spike—

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though that could contribute—but the continual presence of high voltage combined with an insulating material whose comparative tracking index (CTI) is too low.

CTI is a measure of a material as an electrical insulator and is expressed as the voltage at which

the surface of a material breaks down under a standardized test. The manufacturers of

PCB laminates publish CTI figures for their products. For convenience, the breakdown voltages are lumped into six categories: The highest rating is 0 for withstanding values of 600V and greater and the lowest is 5, for less than 100V. For example, conventional FR-4 has a CTI of from 175– 249 volts, which places it in rating category 3.

The paramount objective of all electrical safety standards is of course to prevent any danger of shock. If no one will ever be near a circuit while it is powered, the clearance and creepage allowances among its conductors that are subject to hazardous voltage can be the minimum that ensure the circuit will function and not deteriorate. IEC-60950-1 specifies five increasing levels of mandatory insulation related to the physical location of a circuit relative to human contact, the voltage, and the operating environment. Naturally,

the best tactic to avoid the dan-

ger of shock or circuit degradation is to space traces as far apart as possible but very often that distance will not meet creepage requirements. What can be done in those cases?

If turning to a material with a better CTI is not feasible, routing a slot in the space between

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two traces can increase the creepage distance. Leakage from one trace to the other along the laminate surface would have to travel around the air gap. Alternatively, a vertical barrier of insulating material could be placed in the space, which would increase both the creepage and clearance distances.

Keep in mind the spacing on assembled boards when you consider creepage and clearance requirements for layout. The distance between an uninsulated edge of a charged component and the edge of an adjacent component could be too small to meet a clearance requirement, even though the creepage distance between their traces is sufficient. Moreover, there may be some operations needed during assembly to meet clearance requirements, for example, applying potting compound to isolate the leads on the package of a power semiconductor from a nearby component.

If your project does not require compliance with a particular safety standard, you can rely on the latest version of IPC-2221, the generic standard for PCB design, for clearance and creepage guidance. In any case, consultation with your PCB fabricator and assembler regarding suitable materials and design alternatives will help you achieve a safe product that meets your performance objectives at the lowest possible cost.

Our quick trip through the basics of laying out boards that involve hazardous voltage amounts to just a first step, simply an opportunity to point to out some helpful and hopefully familiar guideposts as you start your journey. Consider this presentation my personal opinion only and certainly not legal advice. **PCBDESIGN** 



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## video Interview

## Printed Circuit Handbook, 7th Ed., Coming Soon

by Real Time with... IPC APEX EXPO



Clyde F. Coombs Jr., editor of the venerable Printed Circuit Handbook, discusses the upcoming 7<sup>th</sup> edition, and what readers can expect. He explains how the book's content has evolved over the years, and why some readers are not "board guys" in the classic sense.

